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PATENT  
Attorney Docket No. ASC-012DV

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

APPLICANTS: Lee et al.  
SERIAL NO.: Not yet assigned      GROUP NO.: Not yet assigned  
FILING DATE: Herewith      EXAMINER: Not yet assigned  
TITLE: STRUCTURES WITH PLANAR STRAINED LAYERS

Mail Stop Patent Application  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**INFORMATION DISCLOSURE STATEMENT**

Sir:

In accordance with the provisions of 37 C.F.R. 1.97 and 1.98, Applicants hereby make of record the patents and publications listed on the accompanying Form PTO-1449, and other information contained herein, which have been submitted for the parent case from which this divisional application depends (divisional of prior application Serial No. 10/211,126, filed on August 2, 2002, which claims the benefit of U.S. Provisional Application No. 60/310,346, filed August 6, 2001). In accordance with the provisions of 37 C.F.R. § 1.98(d), copies of the references are not enclosed as these references were previously submitted to the U.S. Patent and Trademark Office in the parent application but are available upon request.

**REMARKS**

In accordance with the provisions of 37 C.F.R. 1.97, this statement is being filed (CHECK ONE):

- ☒ (1) within three (3) months of the **filing date** of a national application other than a continued prosecution application under 37 C.F.R. 1.53(d), or within three (3) months of the **date of entry of the national stage** as set forth in 37 C.F.R. 1.491 in an international application, or before the mailing of the **first Office action** on the merits, or before the mailing of a **first Office action** after the filing of a request for continued examination under 37 C.F.R. 1.114; or
- ☐ (2) after the period defined in (1) but before the mailing date of a **final action** or a **notice of allowance** under 37 C.F.R. 1.311, and

- ☐ the requisite Statement is below, **OR**
- ☐ the requisite fee under 37 C.F.R. 1.17(p), namely **\$180.00**, is included herein, or
- ☐ (3) after the mailing date of a **final action** or **notice of allowance** but before the payment of the **issue fee**, **AND**
- ☐ the requisite Statement is below, **AND**
- ☐ the requisite petition fee under 37 C.F.R. 1.17(p), namely **\$180.00** is included herein.

It is respectfully requested that each of the patents and publications listed on the attached Form PTO-1449, and other information contained herein, be made of record in this application.

Respectfully submitted,

Date: February 27, 2004  
Reg. No. 44,381

Tel. No.: (617) 310-8327  
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3029581-1



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FORM PTO - 1449	ATTORNEY DOCKET NO.: ASC-012DV
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	SERIAL NO.: Not yet assigned
	FILING DATE: Herewith GROUP: Not yet assigned

## U.S. PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A1	4,710,788	12/01/1987	Dämbkes et al.			
	A2	4,990,979	02/05/1991	Otto			
	A3	5,241,197	08/31/1993	Murakami et al.			
	A4	5,291,439	03/01/1994	Kauffmann et al.			
	A5	5,442,205	08/15/1995	Brasen et al.			
	A6	5,523,592	06/04/1996	Nakagawa et al.			
	A7	5,534,713	07/09/1996	Ismail et al.			

## FOREIGN PATENT DOCUMENTS

EXAM INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
	B1	41 01 167 A1	07/23/1992	DE				No	Yes (abstract only)
	B2	4-307974	10/30/1992	JP				No	No
	B3	7-106446	04/21/1995	JP				No	No
	B4	0 683 522 A2	11/22/1995	EP				No	Yes
	B5	0 829 908 A2	03/18/1998	EP				No	Yes

## OTHER ART, JOURNAL ARTICLES, ETC.

EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)	
	C1	Meyerson et al., "Cooperative Growth Phenomena in Silicon/Germanium Low-Temperature Epitaxy," <u>Applied Physics Letters</u> , Vol. 53, No. 25 (December 19, 1988) pp. 2555-2557.
	C2	Garone et al., "Silicon vapor phase epitaxial growth catalysis by the presence of germane," <u>Applied Physics Letters</u> , Vol. 56, No. 13 (March 26, 1990) pp. 1275-1277.
	C3	Robbins et al., "A model for heterogeneous growth of Si <sub>1-x</sub> Ge <sub>x</sub> films for hydrides," <u>Journal of Applied Physics</u> , Vol. 69, No. 6 (March 15, 1991) pp. 3729-3732.
	C4	"2 Bit/Cell EEPROM Cell Using Band-to-Band Tunneling for Data Read-Out," <u>IBM Technical Disclosure Bulletin</u> , Vol. 35, No. 4B (September 1992) pp. 136-140.
	C5	Wesler et al., "NMOS and PMOS Transistors Fabricated in Strained Silicon/Relaxed Silicon-Germanium Structures," <u>Electron Devices Meeting, 1992. Technical Digest</u> (December 13, 1992) pp. 31.7.1-31.7.3.
	C6	Grützmacher et al., "Ge segregation in SiGe/Si heterostructures and its dependence on deposition technique and growth atmosphere," <u>Applied Physics Letters</u> , Vol. 63, No. 18 (November 1, 1993) pp. 2531-2533.
EXAMINER		DATE CONSIDERED

FORM PTO - 1449	ATTORNEY DOCKET NO.: ASC-012DV
INFORMATION DISCLOSURE STATEMENT	APPLICANTS: Lee et al.
	SERIAL NO.: Not yet assigned
	FILING DATE: Herewith      GROUP: Not yet assigned

## U.S. PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A8	5,596,527	01/12/1997	Tomioka et al.			
	A9	5,617,351	04/01/1997	Bertin et al.			
	A10	5,683,934	11/04/1997	Candelaria			
	A11	5,739,567	04/14/1998	Wong			
	A12	5,777,347	07/07/1998	Bartelink			
	A13	5,786,612	07/28/1998	Otani et al.			
	A14	5,792,679	08/11/1998	Nakato			
	A15	5,808,344	09/15/1998	Ismail et al.			
	A16	5,891,769	04/06/1999	Liaw et al.			
	A17	5,906,951	05/25/1999	Chu et al.			
	A18	5,998,807	12/07/1999	Lustig et al.			

## FOREIGN PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
	B6	0 838 858 A2	04/29/1998	EP				No	Yes
	B7	11-233744	08/27/1999	JP				No	No
	B8	WO 98/59365	12/30/1998	PCT				No	Yes
	B9	WO 99/53539	10/21/1999	PCT				No	Yes
	B10	2001319935	05/2000	JP				Yes	No

## OTHER ART, JOURNAL ARTICLES, ETC.

EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)	
	C7	Welser et al., "Evidence of Real-Space Hot-Electron Transfer in High Mobility, Strained-Si Multilayer MOSFETs," <u>Electron Devices meetings, 1993. Technical Digest</u> (December 1993) pp. 21.3.1-21.3.4.
	C8	Cullis et al., "Growth ripples upon strained SiGe epitaxial layers on Si and misfit dislocation interactions," <u>Journal of Vacuum Science and Technology A</u> , Vol. 12, No. 4 (July/August 1994) pp. 1924-1931.
	C9	Tweet et al., "Factors determining the composition of strained GeSi layers grown with disilane and germane," <u>Applied Physics Letters</u> , Vol. 65, No. 20 (November 14, 1994) pp. 2579-2581.
EXAMINER		DATE CONSIDERED

<b>FORM PTO - 1449</b> <b>INFORMATION DISCLOSURE STATEMENT</b>				ATTORNEY DOCKET NO.: ASC-012DV APPLICANTS: Lee et al. SERIAL NO.: Not yet assigned FILING DATE: Herewith      GROUP: Not yet assigned					
<b>U.S. PATENT DOCUMENTS</b>									
<b>EXAM. INIT.</b>		<b>DOCUMENT NUMBER</b>	<b>DATE</b>	<b>NAME</b>	<b>CLASS</b>	<b>SUB CLASS</b>	<b>FILING DATE IF APPROPRIATE</b>		
	A19	6,013,134	01/11/2000	Chu et al.					
	A20	6,058,044	05/02/2000	Sugiura et al.					
	A21	6,059,895	05/09/2000	Chu et al.					
<b>FOREIGN PATENT DOCUMENTS</b>									
<b>EXAM. INIT.</b>		<b>DOCUMENT NUMBER</b>	<b>DATE</b>	<b>COUNTRY CODE</b>	<b>CLASS</b>	<b>SUB CLASS</b>	<b>FILING DATE</b>	<b>ABSTRACT ONLY</b>	<b>ENGLISH LANG (Y/N)</b>
	B11	1 020 900 A2	07/19/2000	EP				No	Yes
	B12	WO 00/54338	09/14/2000	PCT				No	Yes
	B13	WO 01/54202 A1	07/26/2001	PCT				No	Yes
	B14	WO 01/93338 A1	12/06/2001	PCT				No	Yes
	B15	WO 01/99169 A2	12/27/2001	PCT				No	Yes
	B16	1 174 928 A1	01/23/2002	EP				No	Yes
<b>OTHER ART, JOURNAL ARTICLES, ETC.</b>									
<b>EXAM. INIT.</b>	<b>OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)</b>								
	C10	Armstrong et al., "Design of Si/SiGe Heterojunction Complementary Metal-Oxide-Semiconductor Transistors," <u>IEDM Technical Digest</u> (1995) pp. 761-764.							
	C11	König et al., "SiGe HBTs and HFETs," <u>Solid-State Electronics</u> , Vol. 38, No. 9 (1995) pp. 1595-1602.							
	C12	Rim et al., "Enhanced Hole Mobilities in Surface-Channel Strained-Si p-MOSFETs," <u>Solid State Electronics Laboratory, Stanford University, Stanford, CA 94305</u> (1995) pp. 20.3.1-20.3.4.							
	C13	Welser, "The Application of Strained Silicon/Relaxed Silicon Germanium Heterostructures to Metal-Oxide-Semiconductor Field-Effect Transistors," Ph.D. Thesis, Stanford University (1995) pp. 1-205.							
	C14	Sadek et al., "Design of Si/SiGe Heterojunction Complementary Metal-Oxide-Semiconductor Transistors," <u>IEEE Transactions on Electron Devices</u> , Vol. 43, No. 8 (August 1996) pp. 1224-1232.							
	C15	Nayak et al., "High Mobility Strained-Si PMOSFET's," <u>IEEE Transactions on Electron Devices</u> , Vol. 43, No. 10 (October 1996) pp. 1709-1716.							
	C16	Schäffler, "High-mobility Si and Ge structures," <u>Semicond. Sci. Technol.</u> , Vol. 12 (1997) pp. 1515-1549.							
	C17	Usami et al., "Spectroscopic study of Si-based quantum wells with neighboring confinement structure," <u>Semicon. Sci. Technol.</u> (1997) (abstract).							
<b>EXAMINER</b>					<b>DATE CONSIDERED</b>				

FORM PTO - 1449	ATTORNEY DOCKET NO.: ASC-012DV
INFORMATION DISCLOSURE STATEMENT	APPLICANTS: Lee et al.
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## U.S. PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A22	6,096,590	08/01/2000	Chan et al.			
	A23	6,107,653	08/22/2000	Fitzgerald			
	A24	6,111,267	08/29/2000	Fischer et al.			
	A25	6,117,750	09/12/2000	Bensahel et al.			
	A26	6,130,453	10/10/2000	Mei et al.			
	A27	6,143,636	11/07/2000	Forbes et al.			
	A28	6,204,529	03/20/2001	Lung et al.			
	A29	6,207,977 B1	03/27/2001	Augusto			
	A30	US 2001/0003364 A1	06/14/2001	Sugawara et al.			
	A31	6,249,022	06/19/2001	Lin et al.			
	A32	6,251,755 B1	06/26/2001	Furukawa et al.			
	A33	6,266,278	07/24/2001	Harari et al.			
	A34	US 2002/0100942 A1	08/01/2001	Fitzgerald et al.			
	A35	6,339,232 B1	01/15/2002	Takagi			

## FOREIGN PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
	B17	WO 02/15244A2	02/21/2002	PCT				No	Yes
	B18	WO 02/13262 A2	02/14/2002	PCT				No	Yes
	B19	WO 02/47168 A2	06/13/2002	PCT				No	Yes
	B20	WO 02/071488 A1	09/12/2002	PCT				No	Yes
	B21	WO 02/071491 A1	09/12/2002	PCT				No	Yes

## OTHER ART, JOURNAL ARTICLES, ETC.

EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)	
	C18	König et al., "Design Rules for n-Type SiGe Hetero FETs," <u>Solid State Electronics</u> , Vol. 41, No. 10 (1997), pp. 1541-1547.
	C19	Höck et al., "Carrier mobilities in modulation doped Si <sub>1-x</sub> Ge <sub>x</sub> heterostructures with respect to FET applications," <u>Thin Solid Films</u> , Vol. 336 (1998) pp. 141-144.

EXAMINER	DATE CONSIDERED
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FORM PTO - 1449	ATTORNEY DOCKET NO.: ASC-012DV
INFORMATION DISCLOSURE STATEMENT	APPLICANTS: Lee et al.
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## U.S. PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A36	6,350,993 B1	02/26/2002	Chu et al.			
	A37	US 2002/0125471 A1	09/12/2002	Fitzgerald et al.			12/04/2001
	A38	US 2002/140031 A1	10/03/2002	Rim			03/31/2001
	A39	US 2002/0125497 A1	09/12/2002	Fitzgerald			07/16/2001

## FOREIGN PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
	B22	WO 02/071495 A1	09/12/2002	PCT				No	Yes

## OTHER ART, JOURNAL ARTICLES, ETC.

EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)								
	C20	Maiti et al., "Strained-Si heterostructure field effect transistors," <u>Semicond. Sci. Technol.</u> , Vol. 13 (1998) pp. 1225-1246.							
	C21	Hackbarth et al., "Strain relieved SiGe buffers for Si-based heterostructure field-effect transistors," <u>Journal of Crystal Growth</u> , Vol. 201 (1999) pp. 734-738							
	C22	Armstrong, "Technology for SiGe Heterostructure-Based CMOS Devices," Submitted to the Massachusetts Institute of Technology Department of Electrical Engineering and Computer Science on June 30, 1999, pp. 1-154.							
	C23	O'Neill et al., "SiGe Virtual substrate N-channel heterojunction MOSFETS," <u>Semicond. Sci. Technol.</u> , Vol. 14 (1999) pp. 784-789.							
	C24	Rim, "Application of Silicon Based Heterostructures to Enhanced Mobility Metal-Oxide-Semiconductor Field-Effect Transistors," Ph.D. Thesis, Stanford University (July 1999) pp. 1-184							
	C25	Parker et al., "SiGe heterostructure CMOS circuits and applications," <u>Solid State Electronics</u> , Vol. 43, No. 8, (August 1999) pp. 1497-1506.							

EXAMINER	DATE CONSIDERED
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FORM PTO - 1449	ATTORNEY DOCKET NO.: ASC-012DV
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## OTHER ART, JOURNAL ARTICLES, ETC.

EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)							
	C26	Xie, "SiGe Field effect transistors," <u>Materials Science and Engineering</u> , Vol. 25 (1999) pp. 89-121.						
	C27	Hackbarth et al., "Alternatives to thick MBE-grown relaxed SiGe buffers," <u>Thin Solid Films</u> , Vol. 369, No. 1-2 (2000) pp. 148-151.						
	C28	Herzog et al., "SiGe-based FETs: buffer issues and device results," <u>Thin Solid Films</u> , Vol. 380 (2000) pp. 36-41.						
	C29	Mizuno et al., "Electron and Hole Mobility Enhancement in Strained-Si MOSFET's on SiGe-on-Insulator Substrates Fabricated by SIMOX Technology," <u>IEEE Electron Device Letters</u> , Vol. 21, No. 5 (May 2000) pp. 230-232.						
	C30	Höck et al., "High hole mobility in Si <sub>0.17</sub> Ge <sub>0.83</sub> channel metal-oxide-semiconductor field-effect transistors grown by plasma-enhanced chemical vapor deposition," <u>Applied Physics Letters</u> , Volume 76, No. 26 (June 26, 2000) pp. 3920-3922.						
	C31	Rim et al., "Fabrication and Analysis of Deep Submicron Strained-Si N-MOSFET's," <u>IEEE Transactions on Electron Devices</u> , Vol. 47, No. 7 (July 2000) pp. 1406-1415.						
	C32	Barradas et al., "RBS analysis of MBE-grown Si/Ge(001) Si heterostructures with thin, high Ge content SiGe channels for HMOS transistors," <u>Modern Physics Letters B</u> (2001) (abstract)						
	C33	Cheng et al., "Relaxed Silicon-Germanium on Insulator Substrate by Layer Transfer," <u>Journal of Electronic Materials</u> , Volume 30, No. 12 (2001) pp. L37-L39						
	C34	Lee et al., "Strained Ge channel p-type metal-oxide-semiconductor field-effect transistors grown on Si <sub>1-x</sub> Ge <sub>x</sub> /Si virtual substrates," <u>Applied Physics Letters</u> , Volume 79, No. 20 (November 12, 2001) pp. 3344-3346.						
	C35	Leitz et al., "Hole mobility enhancements in strained Si/Si <sub>1-y</sub> Ge <sub>y</sub> p-type metal-oxide-semiconductor field-effect transistors grown on relaxed Si <sub>1-x</sub> Ge <sub>x</sub> (x<y) virtual substrates," <u>Applied Physics Letters</u> , Volume 79, No. 25 (December 17, 2001) pp. 4246-4248.						
	C36	Canaperi et al., "Preparation of a relaxed Si-Ge layer on an insulator in fabricating high-speed semiconductor devices with strained epitaxial films," <u>Intern. Business Machines Corporation</u> , USA (2002) (abstract).						
EXAMINER				DATE CONSIDERED				

FORM PTO - 1449	ATTORNEY DOCKET NO.: ASC-012DV
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FOREIGN PATENT DOCUMENTS									
EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)

OTHER ART, JOURNAL ARTICLES, ETC.	
EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)
	C37 Lee et al., "Strained Ge channel <i>p</i> -type MOSFETs fabricated on Si <sub>1-x</sub> Ge <sub>x</sub> /Si virtual substrates," <u>Mat. Res. Soc. Symp. Proc.</u> , Volume 686 (2002) pp. A1.9.1-A1.9.5.
	C38 Leitz et al., "Channel Engineering of SiGe-Based Heterostructures for High Mobility MOSFETs," <u>Mat. Res. Soc. Symp. Proc.</u> , Volume 686 (2002) pp. A3.10.1-A3.10.6.
	C39 Li et al., "Design of high speed Si/SiGe heterojunction complementary metal-oxide-semiconductor field effect transistors with reduced short-channel effects," <u>J. Vac. Sci. Technol.</u> , A 20(3) (May/June 2002) pp. 1030-1033.

EXAMINER	DATE CONSIDERED
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OTHER ART, JOURNAL ARTICLES, ETC.									
EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)								
	C40	Eaglesham et al., "Dislocation-Free Stranski-Krastanow Growth of Ge on Si(100)," <u>Physical Review Letters</u> , Vol. 64, No. 16 (April 16, 1990) pp. 1943-1946.							
	C41	Fitzgerald et al., "Totally relaxed $\text{Ge}_x\text{Si}_{1-x}$ layers with low threading dislocation densities grown on Si substrates," <u>Appl. Phys. Lett.</u> , Vol. 59, No. 7 (August 12, 1991) pp. 811-813.							
	C42	Fitzgerald et al., "Relaxed $\text{Ge}_x\text{Si}_{1-x}$ structures for III-V integration with Si and high mobility two-dimensional electron gases in Si," <u>J. Vac. Sci. Technol. B</u> , Volume 10, No. 4 (July/August 1992) pp. 1807-1819.							
	C43	Xie et al., "Very high mobility two-dimensional hole gas in Si/ $\text{Ge}_x\text{Si}_{1-x}$ /Ge structures grown by molecular beam epitaxy," <u>Appl. Phys. Lett.</u> , Vol. 63, No. 16 (October 18, 1993) pp. 2263-2264.							
	C44	Wesler et al., "Electron Mobility Enhancement in Strained-Si N-Type Metal-Oxide-Semiconductor Field-Effect Transistors," <u>IEEE Electron Device Letters</u> , Vol. 15, No. 3 (March 1994) pp. 100-102.							
EXAMINER					DATE CONSIDERED				

<b>FORM PTO - 1449</b>  <b>INFORMATION DISCLOSURE STATEMENT</b>	<b>ATTORNEY DOCKET NO.:</b> ASC-012DV  <b>APPLICANTS:</b> Lee et al.  <b>SERIAL NO.:</b> Not yet assigned  <b>FILING DATE:</b> Herewith <b>GROUP:</b> Not yet assigned
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### OTHER ART, JOURNAL ARTICLES, ETC.

EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)								
	C45	Ismail et al., "Modulation-doped n-type Si/SiGe with inverted interface," <u>Appl. Phys. Lett.</u> , Vol. 65, No. 10 (September 5, 1994) pp. 1248-1250.							
	C46	Xie et al., "Semiconductor Surface Roughness: Dependence on Sign and Magnitude of Bulk Strain," <u>The Physical Review Letters</u> , Vol. 73, No. 22 (November 28, 1994) pp. 3006-3009.							
	C47	Bouillon et al., "Search for the optimal channel architecture for 0.18/0.12 $\mu$ m bulk CMOS Experimental study," <u>IEEE</u> , (1996) pp. 21.2.1-21.2.4.							
	C48	Kearney et al., "The effect of alloy scattering on the mobility of holes in a Si <sub>1-x</sub> Ge <sub>x</sub> quantum well," <u>Semicond. Sci Technol.</u> , Vol. 13 (1998) pp. 174-180.							
	C49	Höck et al., "High performance 0.25 $\mu$ m p-type Ge/SiGe MODFETs," <u>Electronics Letters</u> , Vol. 34, No. 19 (September 17, 1998) pp. 1888-1889.							

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	FILING DATE: Herewith      GROUP: Not yet assigned

U.S. PATENT DOCUMENTS							
EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE

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EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)

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EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)
	C50 Bufler et al., "Hole transport in strained Si <sub>1-x</sub> Ge <sub>x</sub> alloys on Si <sub>1-y</sub> Ge <sub>y</sub> substrates," <u>Journal of Applied Physics</u> , Vol. 84, No. 10 (November 15, 1998) pp. 5597-5602.
	C51 Fitzgerald et al., "Dislocation dynamics in relaxed graded composition semiconductors," <u>Materials Science and Engineering B67</u> , (1999) pp. 53-61.
	C52 Fischetti, "Long-range Coulomb interactions in small Si devices. Part II. Effective electron mobility in thin-oxide structures," <u>Journal of Applied Physics</u> , Vol. 89, No. 2 (January 15, 2001) pp. 1232-1250.
	C53 Cheng et al., "Electron Mobility Enhancement in Strained-Si n-MOSFETs Fabricated on SiGe-on-Insulator (SGOI) Substrates," <u>IEEE Electron Device Letters</u> , Vol. 22, No. 7 (July 2001) pp. 321-323.
	C54 Leitz et al., "Dislocation glide and blocking kinetics in compositionally graded SiGe/Si," <u>Journal of Applied Physics</u> , Vol. 90, No. 6 (September 15, 2001) pp. 2730-2736.
	C55 Currie et al., "Carrier mobilities and process stability of strained S in- and p-MOSFETs on SiGe virtual substrates," <u>J. Vac. Sci. Technol. B</u> , Vol. 19, No. 6 (Nov/Dec 2001) pp. 2268-2279.
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<b>FORM PTO - 1449</b>  <b>INFORMATION DISCLOSURE STATEMENT</b>	ATTORNEY DOCKET NO.: ASC-012DV
	APPLICANTS: Lee et al.
	SERIAL NO.: Not yet assigned
	FILING DATE: Herewith GROUP: Not yet assigned

U.S. PATENT DOCUMENTS							
EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A40	6,399,970 B2	06/04/2002	Kubo et al.			

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EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)

OTHER ART, JOURNAL ARTICLES, ETC.									
EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)								
EXAMINER					DATE CONSIDERED				

FORM PTO - 1449  INFORMATION DISCLOSURE STATEMENT	ATTORNEY DOCKET NO.: ASC-012DV
	APPLICANTS: Lee et al.
	SERIAL NO.: Not yet assigned
	FILING DATE: Herewith      GROUP: Not yet assigned

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	C56	Ransom et al., "Gate-Self-Aligned n-channel and p-channel Germanium MOSFET's," <u>IEEE Transactions on Electron Devices</u> , Vol. 38, No. 12 (December 1991) pp. 2695.						
	C57	König et al., "p-Type Ge-Channel MODFET's with High Transconductance Grown on Si Substrates," <u>IEEE Electron Device Letters</u> , Vol. 14, No. 4 (April 1993) pp. 205-207.						
	C58	Fischetti et al., "Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys," <u>J. Appl. Phys.</u> , Vol. 80, No. 4 (August 15, 1996) pp. 2234-2252.						
	C59	Currie et al., "Controlling threading dislocation densities in Ge on Si using graded SiGe layers and chemical-mechanical polishing," <u>Applied Physics Letters</u> , Vol. 72, No. 14 (April 6, 1998) pp 1718-1720.						
	C60	Reinking et al., "Fabrication of high-mobility Ge p-channel MOSFETs on Si substrates," <u>Electronics Letters</u> , Vol. 35, No. 6 (March 18, 1999) pp. 503-504.						
	C61	Koester et al., "Extremely High Transconductance Ge/Si <sub>0.4</sub> Ge <sub>0.6</sub> p-MODFET's Grown by UHV-CVD," <u>IEEE Electron Device Letters</u> , Vol. 21, No. 3 (March 2000) pp. 110-112.						
	C62	Carlin et al., "High Efficiency GaAs-on-Si Solar Cells with High V <sub>oc</sub> Using Graded GeSi Buffers," <u>IEEE</u> (2000) pp. 1006-1011						
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	APPLICANTS: Lee et al.
	SERIAL NO.: Not yet assigned
	FILING DATE: Herewith
	GROUP: Not yet assigned

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EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE		
	A41	5,780,922	07/14/1998	Mishra et al.					
	A42	5,986,287	11/16/1999	Eberl et al.					
	A43	6,498,359	12/24/2002	Schmidt et al.			05/18/2001		
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EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG Y/N
	B23	63122176	05/26/88	JP				Y	Y
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EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)								
	C63	Reinking et al., "Fabrication of High-Mobility Ge p-Channel MOSFETs on Si Substrates," <u>Electronics Letters</u> , Vol. 35, No. 6 (March 18, 1999) pp. 503-504.							
	C64	Rosenblad et al., "Virtual Substrates for the n- and p-type Si-MODFET Grown at Very High Rates," <u>Materials Science and Engineering</u> , Vol. B74 (2000) pp. 113-117.							
	C65	Ueno et al., "Low Temperature Buffer Growth for Modulation Doped SiGe/Ge/SiGe Heterostructures with High Hole Mobility," <u>Thin Solid Films</u> , Vol. 369 (2000) pp. 320-323.							
	C66	Yousif et al., "Recent Critical Issues in Si/Si <sub>1-x</sub> Ge <sub>x</sub> /Si Heterostructure FET Devices," <u>Solid-State Electronics</u> , Vol. 45, No. 11 (2001) pp. 1931-1937.							
	C67	Anonymous, "Germanium P-Channel Mosfet," <u>IBM Technical Disclosure Bulletin</u> , Vol. 28, No. 2 (July 1, 1985) p. 500.							
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	APPLICANTS: Lee et al.
	SERIAL NO.: Not yet assigned
	FILING DATE: Herewith      GROUP: Not yet assigned

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EXAM. INIT.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE

## FOREIGN PATENT DOCUMENTS

EXAM. INIT.	DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)

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	C68	Aigouy et al., "MOVPE Growth and optical characterization of ZnSe/ZnS strained layer superlattices," <u>Superlattices and Microstructures</u> , Vol. 16, No. 1 (1994) pp. 71-76
	C69	Kikkawa et al., "Effect of strained InGaAs step bunching on mobility and device performance in n-InGaP/InGaAs/GaAs pseudomorphic heterostructures grown by metalorganic vapor phase epitaxy," <u>Journal of Crystal Growth</u> , Vol. 145 (1994) pp. 799-807.
	C70	Pelekanos et al., "Interface roughness correlation in CdTe/CdZnTe strained quantum wells," <u>Journal of Crystal Growth</u> , Vol. 184/185 (1998) pp. 886-889.
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APPLICANTS: Lee et al.

SERIAL NO.: Not yet assigned

FILING DATE: Herewith

GROUP: Not yet assigned

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EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A44	5,963,817	10/05/1999	Chu et al.			
	A45	2002/0100942	08/01/2002	Fitzgerald et al.			
	A46	2002/0123197	09/05/2002	Fitzgerald et al.			06/19/2001
	A47	2002/0125471	09/12/2002	Fitzgerald et al.			12/04/2001
	A48	2002/0125497	09/12/2002	Fitzgerald			07/16/2001
	A49	2002/0197803	12/26/2002	Leitz et al.			06/21/2002
	A50	2003/0013323	01/16/2003	Hammond et al.			06/14/2002
	A51	2003/0052334	03/20/2003	Lee et al.			06/18/2002

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EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
	B24	02241195	08/28/2002	JP			02/15/2001	NO	YES

## OTHER ART, JOURNAL ARTICLES, ETC.

EXAM.  
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OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)


EXAMINER

DATE CONSIDERED

<b>FORM PTO - 1449</b>  <b>INFORMATION DISCLOSURE STATEMENT</b>	ATTY DOCKET NO.:	ASC-012DV
	APPLICANTS:	Lee et al.
	SERIAL NO.:	Not yet assigned
	FILING DATE:	Herewith
	GROUP:	Not yet assigned

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EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A52	2003/0057439	03/27/2003	Fitzgerald			08/09/2002
	A53	2003/0077867	04/24/2003	Fitzgerald			07/16/2001
	A54	2003/0089901	05/15/2003	Fitzgerald			07/16/2001
	A55	09/906,545	07/16/2001	Fitzgerald			
	A56	09/906,200	07/16/2001	Fitzgerald			
	A57	10/164,665	06/07/2002	Currie et al.			

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EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)

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EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)	
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<b>FORM PTO - 1449</b>  <b>INFORMATION DISCLOSURE STATEMENT</b>	<b>ATTY DOCKET NO.:</b>	ASC-012DV
	<b>APPLICANTS:</b>	Lee et al.
	<b>SERIAL NO.:</b>	Not yet assigned
	<b>FILING DATE:</b>	Herewith
	<b>GROUP:</b>	Not yet assigned

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	A58	4,920,076	04/24/1990	Holland et al.			
	A59	5,312,766	05/17/1994	Aronowitz et al.			
	A60	5,327,375	07/05/1994	Harari			

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EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
	B25	0 844 651 A1	05/27/1998	EP				NO	YES

**OTHER ART, JOURNAL ARTICLES, ETC.**

EXAM. INIT.	<b>OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)</b>	
<b>EXAMINER</b>		
<b>DATE CONSIDERED</b>		

FORM PTO - 1449  INFORMATION DISCLOSURE STATEMENT	ATTORNEY DOCKET NO.: ASC-012DV
	APPLICANTS: Lee et al.
	SERIAL NO.: Not yet assigned
	FILING DATE: Herewith      GROUP: Not yet assigned

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EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE

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EXAM INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)

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	C71	Srolovitz, "On the Stability of Surfaces of Stressed Solids," <u>Acta metall.</u> , Vol. 37, No. 2 (1989) pp. 621-625.
	C72	Cullis et al, "The characteristics of strain-modulated surface undulations formed upon epitaxial Si <sub>1-x</sub> Ge <sub>x</sub> alloy layers on Si," <u>Journal of Crystal Growth</u> , Vol 123 (1992) pp. 333-343.

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<b>FORM PTO - 1449</b>  <b>INFORMATION DISCLOSURE STATEMENT</b>				<b>ATTORNEY DOCKET NO.:</b> ASC-012DV  <b>APPLICANTS:</b> Lee et al.  <b>SERIAL NO.:</b> Not yet assigned  <b>FILING DATE:</b> Herewith <b>GROUP:</b> Not yet assigned					
<b>U.S. PATENT DOCUMENTS</b>									
<b>EXAM. INIT.</b>		<b>DOCUMENT NUMBER</b>	<b>DATE</b>	<b>NAME</b>	<b>CLASS</b>	<b>SUB CLASS</b>	<b>FILING DATE IF APPROPRIATE</b>		
	A61	5,461,243	10/24/1995	Ek et al.					
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<b>EXAM INIT.</b>		<b>DOCUMENT NUMBER</b>	<b>DATE</b>	<b>COUNTRY CODE</b>	<b>CLASS</b>	<b>SUB CLASS</b>	<b>FILING DATE</b>	<b>ABSTRACT ONLY</b>	<b>ENGLISH LANG (Y/N)</b>
<b>OTHER ART, JOURNAL ARTICLES, ETC.</b>									
	C73	Wolf et al., "Silicon Processing for the VLSI Era, Volume 1: Process Technology" (1986) pp. 201.							
<b>EXAMINER</b>					<b>DATE CONSIDERED</b>				

<b>FORM PTO - 1449</b>  <b>INFORMATION DISCLOSURE STATEMENT</b>	ATTORNEY DOCKET NO.: ASC-012DV
	APPLICANTS: Lee et al.
	SERIAL NO.: Not yet assigned
	FILING DATE: Herewith      GROUP: Not yet assigned

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EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A62	5,847,419	12/08/1998	Imai et al.			

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EXAM INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)

### OTHER ART, JOURNAL ARTICLES, ETC.

<b>EXAMINER</b>		<b>DATE CONSIDERED</b>

<b>FORM PTO - 1449</b>  <b>INFORMATION DISCLOSURE STATEMENT</b>				<b>ATTORNEY DOCKET NO.:</b> ASC-012DV  <b>APPLICANTS:</b> Lee et al.  <b>SERIAL NO.:</b> Not yet assigned  <b>FILING DATE:</b> Herewith  <b>GROUP:</b> Not yet assigned			
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EXAM. INIT.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE	
	A63	5,847,419	12/08/1998	Imai et al.			
	A64	6,593,191	07/15/2003	Fitzgerald			05/16/2001
	A65	6,600,170	07/29/2003	Xiang			12/17/2001

  

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EXAM. INIT.	DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)	

  

OTHER ART, JOURNAL ARTICLES, ETC.		
EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)	
	C73	International Search Report for PCT/US03/17275, dated October 14, 2003.

  

<b>EXAMINER</b>	<b>DATE CONSIDERED</b>
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FORM PTO - 1449  INFORMATION DISCLOSURE STATEMENT	ATTY DOCKET NO.:	ASC-012DV
	APPLICANTS:	Lee et al.
	SERIAL NO.:	Not yet assigned
	FILING DATE:	Herewith
	GROUP:	Not yet assigned

U.S. PATENT DOCUMENTS							
EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A66	5,155,571	10/13/1992	Wang et al.			
	A67	6,407,406	06/18/2002	Tezuka			
	A68	6,555,839	04/29/2003	Fitzgerald			05/16/2001
	A69	6,583,437	06/24/2003	Mizuno et al.			03/19/2001
	A70	6,593,641	07/15/2003	Fitzgerald			07/16/2001
	A71	6,649,480	11/18/2003	Fitzgerald et al.			06/19/2001
	A72	2003/0052334	03/20/2003	Lee et al.			06/18/2002

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EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
	B26	9-219524	08/19/1997	JP				No	Yes, Abstract Only
	B27	2000-21783	01/21/2000	JP				No	Yes, Abstract Only
	B28	2001-160594	06/12/2001	JP				No	Yes, Abstract Only
	B29	2001-168342	06/22/2001	JP				No	Yes, Abstract Only

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EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)	
	C73	Yeo et al., "Enhanced Performance in Sub-100 nm CMOSFETs Using Strained Epitaxial Silicon-Germanium" IEEE, <u>Proceedings of IEDM Conference 2000, Piscataway, New Jersey, (December 10, 2000)</u> pp. 753-756.
	C74	Mizuno et al., "Advanced SOI-MOSFETs with Strained-Si Channel for High Speed CMOS Electron/Hole Mobility Enhancement," <u>2000 Symposium on VLSI Digest of Technology Papers</u> (June 13, 2000) pp. 210-211.
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